

Application No. 09/992,637

UNMT 1000-1

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A data processing system, comprising:

a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle;

a plurality of routing units, responsive to respective routing control signals and coupled to the plurality of functional units, by which data is steered among inputs and outputs of the plurality of functional units, ~~the routing control signals indicating a source functional unit and a destination functional unit for a data unit; and~~

control word ~~logic~~ distribution circuitry which supplies control words the routing control signals in parallel to the plurality of routing units to establish a route for a function cycle; ~~said control words including the routing control signals.~~

2. (original) The data processing system of claim 1, wherein said plurality of routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.

3. (original) The data processing system of claim 1, wherein said plurality of routing units includes at least one crossbar switch.

4. (original) The data processing system of claim 1, wherein said plurality of functional units includes at least one storage element.

5. (currently amended) The data processing system of claim 1, wherein said plurality of functional units includes at least one logic block which performs a plurality of available

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functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the ~~control word~~.

6. (currently amended) The data processing system of claim 1, wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the ~~control word includes~~ control word distribution circuitry supplies at least one of the write control signals and read control signals.

7. (currently amended) The data processing system of claim 6, wherein ~~said control word includes~~ the control word distribution circuitry supplies an address for said memory.

8. (original) The data processing system of claim 6, wherein an address for said memory is supplied by one of the plurality of functional units.

9. (original) The data processing system of claim 1, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

10. (original) The data processing system of claim 1, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

11. (currently amended) The data processing system of claim 1, wherein said control word logic distribution circuitry supplies said control words routing control signals synchronously to the plurality of functional units.

12. (currently amended) A data processing system, comprising:

a plurality of processing blocks having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a function cycle;

a plurality of routing units, coupled to the plurality of processing blocks and responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the inputs and outputs of the plurality of processing blocks; and

block level control word logic distribution circuitry which supplies signals control words

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for respective function cycles to the plurality of routing units, said control words including the routing control signals for the plurality of routing units processing blocks; wherein processing blocks in said plurality of processing blocks respectively include

a plurality of functional units having respective inputs and outputs, and adapted to perform respective processes using input data at the respective inputs and to supply output data at the respective outputs, within a block function cycle;

a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of functional unit level routing units, by which data is steered among the inputs and outputs of the plurality of functional units; and

functional unit level control word logic distribution circuitry which supplies signals control words for respective block function cycles to the plurality of unit level routing units, said control words including the routing control signals for the plurality of functional unit level routing units.

13. (original) The data processing system of claim 12, wherein said plurality of unit level routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.

14. (original) The data processing system of claim 12, wherein said plurality of block level routing units includes at least one crossbar switch.

15. (original) The data processing system of claim 12, wherein said plurality of functional units includes at least one storage element.

16. (original) The data processing system of claim 12, wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the control word.

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17. (currently amended) The data processing system of claim 12, wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the function unit level control word distribution circuitry supplies includes at least one of the write control signals and read control signals.

18. (currently amended) The data processing system of claim 17, wherein said function unit level control word distribution circuitry supplies includes an address for said memory.

19. (original) The data processing system of claim 17, wherein an address for said memory is supplied by one of the plurality of functional units.

20. (original) The data processing system of claim 12, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

21. (original) The data processing system of claim 12, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

22. (currently amended) The data processing system of claim 12, wherein at least one of said block level control word logic distribution circuitry and functional level control word logic supplies distribution circuitry supplies said control words synchronously.

23. (currently amended) A method of processing data, in a data processing engine that includes a plurality of functional units, comprising:

providing a set of software ~~control words that~~ routing control signals in parallel to a set of routing units in the data processing engine to specify a route among the plurality of functional units; and

routing data among the plurality of functional units according to the set of software ~~control words~~ routing control signals and performing tasks in the plurality of functional units using the route to produce a result.

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24. (currently amended) The method of claim 21 ~~23~~, including:

compiling a high level programming language specifying the result to produce the set of software ~~control~~ words routing control signals.

25. (currently amended) The method of claim ~~24~~ 23, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

26. (currently amended) The method of claim ~~24~~ 23, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

27. (currently amended) The method of claim ~~24~~ 23, wherein the routing units in the data processing engine ~~comprises~~ comprise a plurality of switches interconnecting the plurality of functional units, and said ~~first and second sets set of control words~~ routing control signals specify data paths through the plurality of switches.

28. (original) The method of claim 23, including synchronously routing said data among the plurality of functional units.

29. (currently amended) A method of processing data, in a data processing engine that includes a plurality of functional units, comprising;

providing a first set of software ~~control words~~ routing control signals ~~that in parallel to a set of routing units in the data processing engine~~ to specify a first data path according to a first configuration of the plurality of functional units; and

performing tasks in said plurality of functional units using the first data path;

providing a second set of software control words routing control signals ~~that in parallel to said set of routing units to specifies~~ specify a second data path according to a second configuration of the plurality of functional units, whereby the plurality of functional units is reconfigured to perform a different function; and

performing tasks in said plurality of functional units using the second data path to accomplish said different function.

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30. (original) The method of claim 29, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

31. (original) The method of claim 29, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

32. (currently amended) The method of claim 29, wherein the routing units in the data processing engine comprises a plurality of switches interconnecting the plurality of functional units, and said first and second sets of control words routing control signals specify data paths through the plurality of switches.

33. (currently amended) The method of claim 29, including:

compiling a high level programming language specifying the result to produce the first and second sets of software control ~~words~~ routing control signals.

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